



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,893	03/10/2004	Makoto Noda	7217/71823	8319
7590 09/22/2004			EXAMINER	
JAY H. MAIOLI Cooper & Dunham LLP 1185 Avenue of the Americas New York, NY 10036			YOUNG, BRIAN K	
			ART UNIT	PAPER NUMBER
			2819	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/799,893	NODA ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 July 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-14 is/are allowed.
- 6) ☒ Claim(s) 15-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

Art Unit: 2819

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Ko.

Ko discloses an apparatus for modulating input data by encoding the data to a run length limited (RLL) code data satisfying the (d,k,m,n) condition and decoding the modulated data, in which d is a minimum run length, k is a maximum run length, m is the bit number of input code data, n is the bit number of transmission code data, and the encoding and decoding apparatus according to the present invention comprises a look-up table (LUT) for encoding input parallel m-bit code data to r-bit code data in which r is not less than m and less than n, a post-*encoder* for encoding the encoded r-bit data to an n-bit transmission code data, a pre-decoder for decoding the input n-bit transmission code data to the r-bit code data according to the minimum run length condition, and a LUT for decoding the decoded r-bit code data to the original m-bit code data, by which the transmission code length is shortened according to the minimum run length condition so that the memory size required for encoding and decoding RLL code data can be reduced.

FIG. 8 illustrates an embodiment of the encoding apparatus according to the invention for (2,12,8,15) code data, which is described below with reference to FIG. 9. According to FIG. 8, the S/P converter 110 converts serial 8-bit code data into parallel 8-bit code data, and then transmits the serial 8-bit code data to the LUT 120. The LUT 120 receives the parallel 8-bit data and outputs 10-bit coded data. For example, assuming that the encoded RLL transmission data for output should be "000100010001001" when the parallel 8-bit data input to the LUT 120 satisfying the

Art Unit: 2819

condition of  $(d,k,m,n)=(2,12,8,15)$  is xxxxxxxx, the LUT 120 is constituted so that the output of the LUT 120 becomes "0011100101" of a 10-bit word length for transmission to the five 2-to-3 mappers 131-135 in the post-**encoder** 130 instead of being transmitted as "000100010001001" of a 15-bit word length for direct output.

Here, the mapping table of the 2-to-3 mapper is constructed in a reverse configuration of Table 2 in which the corresponding inputs and outputs in Table 2 are respectively exchanged, and the 2-to-3 mapper comprises a simple logic circuit as shown in FIG. 9. According to FIG. 9, the AND gate G31 logically multiplies each bit of the 2-bit data transmitted from the LUT 120, i.e., MSB and LSB, and then outputs the result thereof as the MSB of the 3-bit code data for output. The AND gate G33 logically multiplies the output of the inverter G32 for inverting the output of the AND gate G31 and the MSB of the 2-bit data transmitted from the LUT 120, and then outputs the results thereof as the second bit of the 3-bit for output. The AND gate G34 logically multiplies the output of the inverter G32 and the LSB of the 2-bit data transmitted from the LUT 120, and then outputs the result thereof as the LSB of the 3-bit data for output.

The post-**encoder** 130 encodes the 10-bit code data transmitted from the LUT 120 into such 15-bit transmission code data as "000100010001001," and then transmits the 15-bit code data to the P/S inverter 140 for final output.

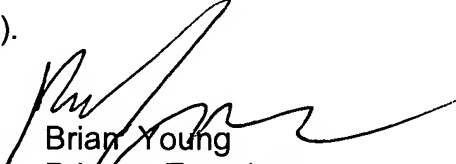
3. Claims 1-14 are allowed.

Art Unit: 2819

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Brian Young  
Primary Examiner  
Art Unit 2819

\*\*\*